CLAIMS:

1. An arrangement for testing integrated circuits, including
- a test system (2) which includes a test vector generator (4) for generating test vectors, and
- a logic component (8) which is included in the integrated circuit (1) to be tested.

2. An arrangement as claimed in claim 1, characterized in that the integrated circuit (1) to be tested includes a test response analysis unit (5) for compressing test response vectors, and a test control block (6) for controlling the test procedure.

3. An arrangement as claimed in claim 1, characterized in that the test vector generator (4) in the test system (2) is arranged to generate the test vectors that are intended to be transferred to the integrated circuit (1) to be tested.

4. An arrangement as claimed in claim 1, characterized in that the test response analysis unit (5) is included in the test system (2) and is arranged to compress the test response vectors to be received from the integrated circuit (1) to be tested.

5. An arrangement a claimed in claim 1, characterized in that the test system (2) includes a programmable algorithmic test vector generator (4) which includes an arithmetic and logic unit (ALU) and generates test vectors in real time.

6. A method of testing logic circuits wherein test vectors that are generated by a programmable algorithmic test vector generator (4) which is included in a test system (2) are transferred to a circuit (1) to be tested which includes a logic component (8) to be tested, and wherein the test response vectors are compressed by means of a test response analysis unit (5) and the compressed test response vectors are evaluated by the test system (2).

7. An integrated circuit (1) which includes a test response analysis unit (5) and a test control block (6), wherein a circuit (1) to be tested is arranged to receive test vectors which are generated by a programmable algorithmic test vector generator (4) which is

included in a test system (2), and to generate test response vectors, the test response analysis unit (5) being arranged to compress the test responses under the control of the test control block (6).

8. A test system (2) which includes a programmable algorithmic test vector generator (4) for generating test vectors which are intended to be applied to a circuit (1) to be tested, the test system (2) being arranged to receive and evaluate test response vectors supplied by the circuit (1) to be tested.

9. A test system as claimed in claim 8, characterized in that a test response analysis unit (5) for compressing test response vectors supplied by the circuit (1) to be tested is integrated in the test system (2) which evaluates the compressed test response vectors.